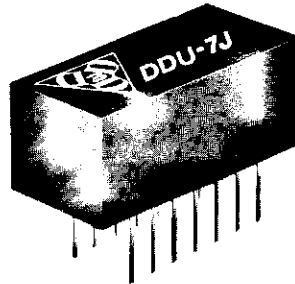


# Digital Delay Units

**SERIES DDU-7J**

**10 Taps (14 pins DIP)  
T<sup>2</sup>L Interfaced**

**data  
delay  
devices, inc.**



(Commercial Type)

## Features:

- Completely interfaced for TTL and DTL application
- No external components required
- P.C. board space economy achieved
- Fits standard 14 pins DIP socket
- Operates over commercial temperature range

## Specifications:

- No. Taps: 10 equally spaced taps
- Total Delay Tolerance:  $\pm 5\%$  or better, or 2 ns whichever is greater.
- Rise-time: 4 ns typically
- Temperature coefficient: 100 PPM/ $^{\circ}\text{C}$ .
- Temperature range:  $0^{\circ}$  to  $+70^{\circ}\text{C}$
- Supply voltage: 4.5 to 5.5 Vdc.
- Logic 1 input current: 100  $\mu\text{a}$  max.
- Logic 0 input current:  $-4$  ma. max.
- Logic 1 V out: 2.5 V min.
- Logic 0 V out: 0.5 V max.
- Logic 1 Fan-out: 20/tap max.
- Logic 0 Fan-out: 10/tap max.
- Power Dissipation: 740 mw max.

## Test Conditions:

- Input Pulse Width:  $\geq 150\%$  of total delay.
- Time delay measured @ 1.5 V on rising edge.
- Unless otherwise specified all time-delays are referenced to input of delay line.
- Rise-time is measured from .75 V to 2.4 V of leading edge.
- All measurements made @  $V_{cc} = 5\text{V}$ ;  $T_A = +25^{\circ}\text{C}$ .

Part No.	Total Delay (ns)	Delay Per Tap (ns)
*DDU-7J-10	9	1 $\pm$ .4
*DDU-7J-20	18	2 $\pm$ .5
*DDU-7J-25	22.5	2.5 $\pm$ .7
*DDU-7J-50	45	5.0 $\pm$ 1.5
DDU-7J-100	100	10.0 $\pm$ 2
DDU-7J-150	150	15.0 $\pm$ 2
DDU-7J-200	200	20.0 $\pm$ 2
DDU-7J-250	250	25.0 $\pm$ 2
DDU-7J-300	300	30.0 $\pm$ 3
DDU-7J-400	400	40.0 $\pm$ 4
DDU-7J-500	500	50.0 $\pm$ 5

\*Time delay referenced to 1st tap. Two (2) gates in parallel for input buffer.

