

# 5-TAP, HCMOS-INTERFACED FIXED DELAY LINE (SERIES DDU8C)

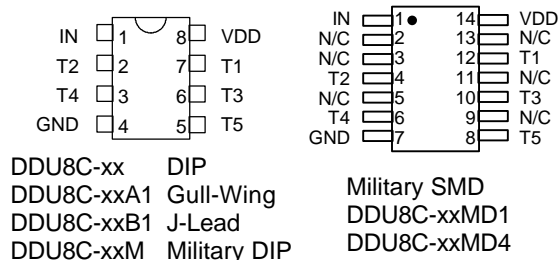
**data  
delay  
devices, inc.**



## FEATURES

- Five equally spaced outputs
- Fits standard 8-pin DIP socket
- Low profile
- Auto-insertable
- Input & outputs fully CMOS interfaced & buffered
- 10 T<sup>2</sup>L fan-out capability

## PACKAGES



## FUNCTIONAL DESCRIPTION

The DDU8C-series device is a 5-tap digitally buffered delay line. The signal input (IN) is reproduced at the outputs (T1-T5), shifted in time by an amount determined by the device dash number (See Table). The total delay of the line is measured from IN to T5. The nominal tap-to-tap delay increment is given by one-fifth of the total delay.

## PIN DESCRIPTIONS

IN Signal Input  
T1-T5 Tap Outputs  
VDD +5 Volts  
GND Ground

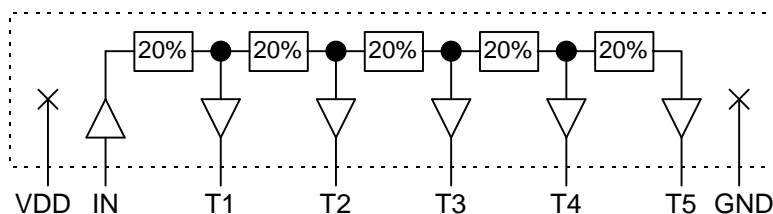
## SERIES SPECIFICATIONS

- **Minimum input pulse width:** 40% of total delay
- **Output rise time:** 8ns typical
- **Supply voltage:** 5VDC  $\pm$  5%
- **Supply current:**  $I_{CCL} = 40\mu\text{a}$  typical  
 $I_{CCH} = 10\text{ma}$  typical
- **Operating temperature:** 0° to 70° C
- **Temp. coefficient of total delay:** 300 PPM/°C

## DASH NUMBER SPECIFICATIONS

Part Number	Total Delay (ns)	Delay Per Tap (ns)
DDU8C-5050	50 $\pm$ 2.5	10.0 $\pm$ 3.0
DDU8C-5060	60 $\pm$ 3.0	12.0 $\pm$ 3.0
DDU8C-5075	75 $\pm$ 4.0	15.0 $\pm$ 3.0
DDU8C-5100	100 $\pm$ 5.0	20.0 $\pm$ 3.0
DDU8C-5125	125 $\pm$ 6.5	25.0 $\pm$ 3.0
DDU8C-5150	150 $\pm$ 7.5	30.0 $\pm$ 3.0
DDU8C-5175	175 $\pm$ 8.0	35.0 $\pm$ 4.0
DDU8C-5200	200 $\pm$ 10.0	40.0 $\pm$ 4.0
DDU8C-5250	250 $\pm$ 12.5	50.0 $\pm$ 5.0

**NOTE:** Any dash number between 5004 and 5250 not shown is also available.



**DDU8C Functional diagram**

## APPLICATION NOTES

### HIGH FREQUENCY RESPONSE

The DDU8C tolerances are guaranteed for input pulse widths and periods greater than those specified in the test conditions. Although the device will function properly for pulse widths as small as 40% of the total delay and periods as small as 80% of the total delay (for a symmetric input), the delays may deviate from their values at low frequency. However, for a given input condition, the deviation will be repeatable from pulse to pulse. Contact technical support at Data

Delay Devices if your application requires device testing at a specific input condition.

### POWER SUPPLY BYPASSING

The DDU8C relies on a stable power supply to produce repeatable delays within the stated tolerances. A 0.1 $\mu$ f capacitor from VDD to GND, located as close as possible to the VDD pin, is recommended. A wide VDD trace and a clean ground plane should be used.

## DEVICE SPECIFICATIONS

**TABLE 1: ABSOLUTE MAXIMUM RATINGS**

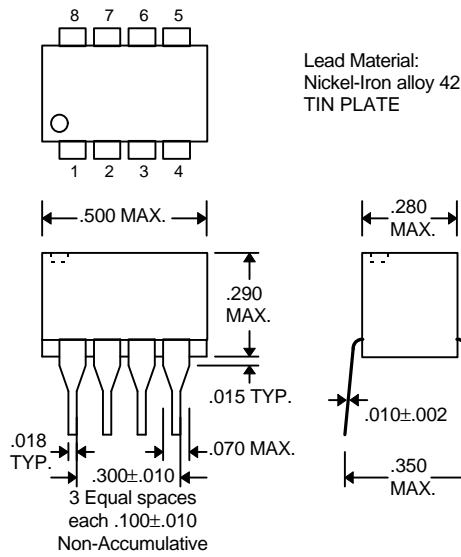
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	$V_{DD}$	-0.3	7.0	V	
Input Pin Voltage	$V_{IN}$	-0.3	$V_{DD}+0.3$	V	
Storage Temperature	$T_{STRG}$	-55	150	C	
Lead Temperature	$T_{LEAD}$		300	C	10 sec

**TABLE 2: DC ELECTRICAL CHARACTERISTICS**

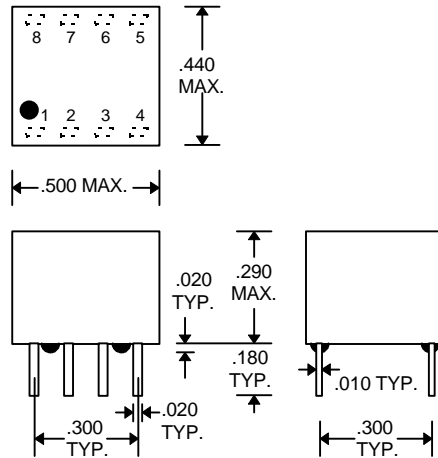
(0C to 70C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
High Level Output Voltage	$V_{OH}$	3.98	4.4		V	$V_{DD} = 5.0$ , $I_{OH} = MAX$ $V_{IH} = MIN$ , $V_{IL} = MAX$
Low Level Output Voltage	$V_{OL}$		0.15	0.26	V	$V_{DD} = 5.0$ , $I_{OL} = MAX$ $V_{IH} = MIN$ , $V_{IL} = MAX$
High Level Output Current	$I_{OH}$			-4.0	mA	
Low Level Output Current	$I_{OL}$			4.0	mA	
High Level Input Voltage	$V_{IH}$	3.15			V	
Low Level Input Voltage	$V_{IL}$			1.35	V	
Input Current	$I_{IH}$			0.10	$\mu$ A	$V_{DD} = 5.0$

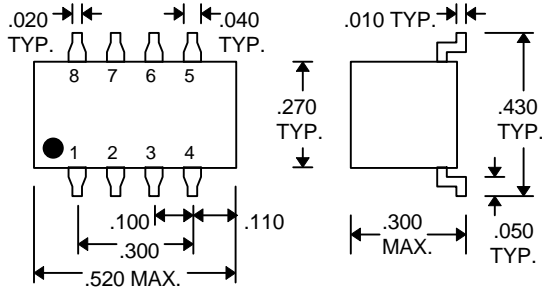
PACKAGE DIMENSIONS



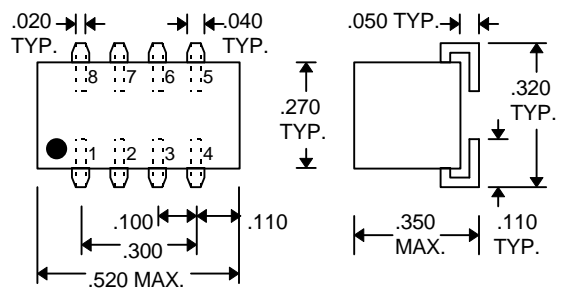
DDU8C-xx (Commercial DIP)



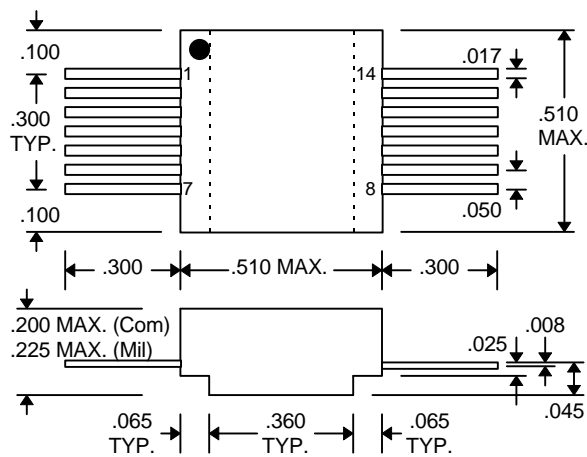
DDU8C-xxM (Military DIP)



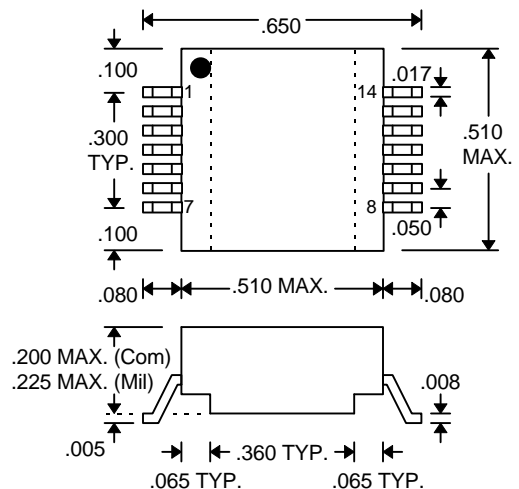
DDU8C-xxA1 (Commercial Gull-Wing)



DDU8C-xxB1 (Commercial J-Lead)



DDU8C-xxD1 (Commercial SMD)  
DDU8C-xxMD1 (Military SMD)



DDU8C-xxD4 (Commercial SMD)  
DDU8C-xxMD4 (Military SMD)

## DELAY LINE AUTOMATED TESTING

### TEST CONDITIONS

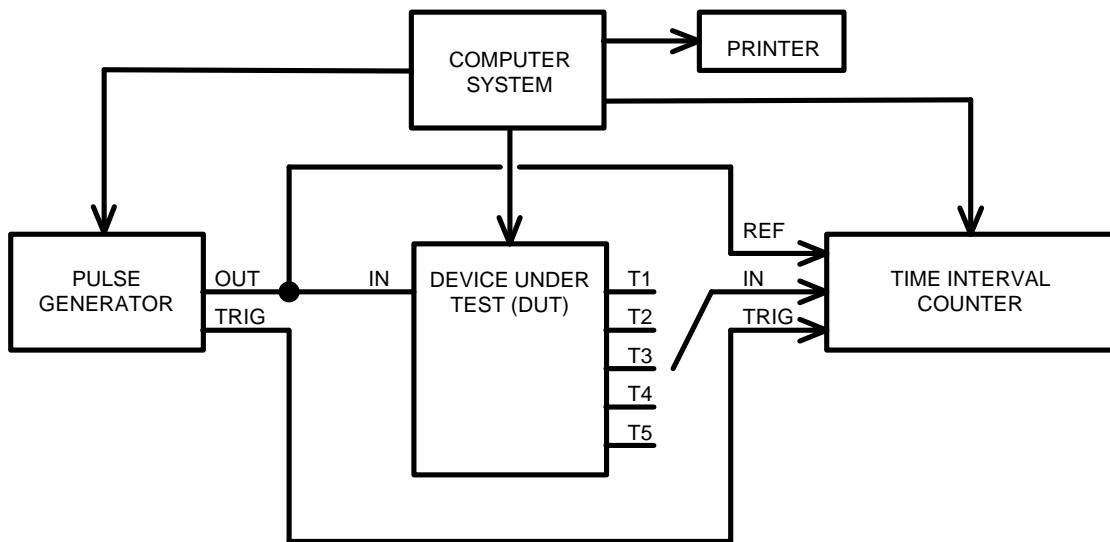
**INPUT:**

**Ambient Temperature:**  $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$   
**Supply Voltage (VDD):**  $5.0\text{V} \pm 0.1\text{V}$   
**Input Pulse:** High =  $5.0\text{V} \pm 0.1\text{V}$   
 Low =  $0.0\text{V} \pm 0.1\text{V}$   
**Source Impedance:**  $50\Omega$  Max.  
**Rise/Fall Time:**  $5.0\text{ ns}$  Max. (measured between  $0.5\text{V}$  and  $4.5\text{V}$ )  
**Pulse Width:**  $\text{PW}_{\text{IN}} = 1.5 \times \text{Total Delay}$   
**Period:**  $\text{PER}_{\text{IN}} = 10 \times \text{Total Delay}$

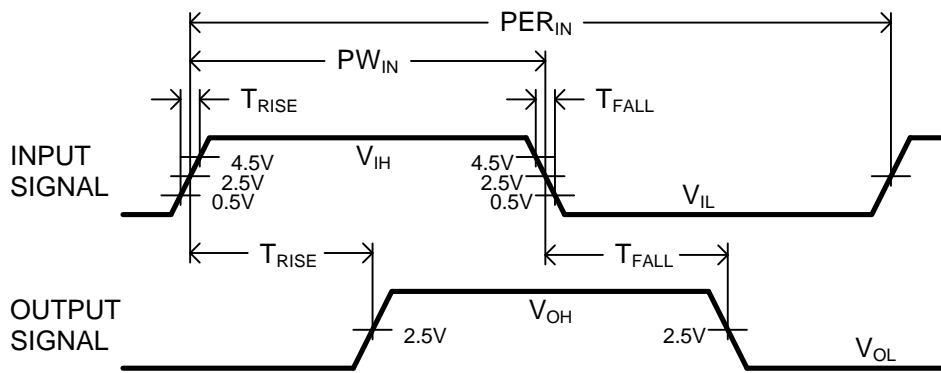
**OUTPUT:**

**Load:** 1 FAST-TTL Gate  
**C<sub>load</sub>:**  $5\text{pf} \pm 10\%$   
**Threshold:**  $2.5\text{V}$  (Rising & Falling)

**NOTE:** The above conditions are for test only and do not in any way restrict the operation of the device.



**Test Setup**



**Timing Diagram For Testing**