MONOLITHIC MANCHESTER ENCODER (SERIES 3D3521)

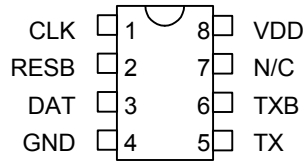
RoHS Compliant

data delay devices, inc.

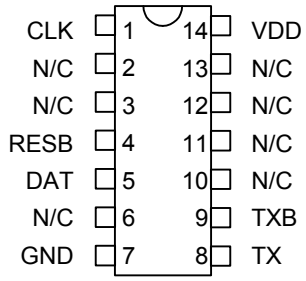
FEATURES

- All-silicon, low-power CMOS technology
- 3.3V operation
- CMOS compatible inputs and outputs
- Vapor phase, IR and wave solderable
- Low ground bounce noise
- **Maximum data rate:** 50 MBaud

PACKAGES



3D3521Z SOIC (.150)



3D3521D SOIC (.150)

For mechanical dimensions, click here.
For package marking details, click here.

FUNCTIONAL DESCRIPTION

The 3D3521 is a monolithic CMOS Manchester Encoder. The clock and data, present at the unit input, are combined into a single bi-phase-level signal. In this encoding mode, a logic one is represented by a high-to-low transition within the bit cell, while a logic zero is represented by a low-to-high transition. The unit operating baud rate (in Mbaud) is equal to the input clock frequency (in MHZ). All pins marked N/C must be left unconnected.

PIN DESCRIPTIONS

DAT	Data Input
CLK	Clock Input
RESB	Reset
TX	Signal Output
TXB	Inverted Signal Output
VDD	+3.3 Volts
GND	Ground

The all-CMOS 3D3521 integrated circuit has been designed as a reliable, economic alternative to hybrid Manchester Encoders. It is CMOS-compatible and is offered in space saving surface mount 8-pin and 14-pin SOICs.

APPLICATION NOTES

The 3D3521 Manchester Encoder samples the data input at the rising edge of the input clock. The sampled data is used in conjunction with the clock rising and falling edges to generate the by-phase level Manchester code.

INPUT SIGNAL CHARACTERISTICS

The 3D3521 Manchester Encoder inputs **are CMOS compatible. The user should assure himself that** the 50% (of VDD) threshold is used when referring to all timing, especially to the input clock duty cycle.

CLOCK DUTY CYCLE ERRORS

The 3D3521 Manchester Encoder employs the timing of the clock rising and falling edges (duty cycle) to implement the required coding scheme. To reduce the difference between the output data high time and low time, it is essential that the deviation of the input clock duty cycle from 50/50 be minimized.

OUTPUT SIGNAL CHARACTERISTICS

The 3D3521 presents at its outputs the true and the complimented encoded data.

The High-to-Low time skew of the selected data output should be budgeted by the user, as it relates to his application, to satisfactorily estimate the distortion of the transmitted data stream.

Such an estimate is very useful in determining the
functionality and margins of the data link, if a 3D3522 Manchester Decoder is used to decode the received data.

POWER SUPPLY AND TEMPERATURE CONSIDERATIONS

CMOS integrated circuitry is strongly dependent on power supply and temperature. The monolithic 3D3521 Manchester encoder utilizes novel and innovative compensation circuitry to minimize timing variations induced by fluctuations in power supply and/or temperature.

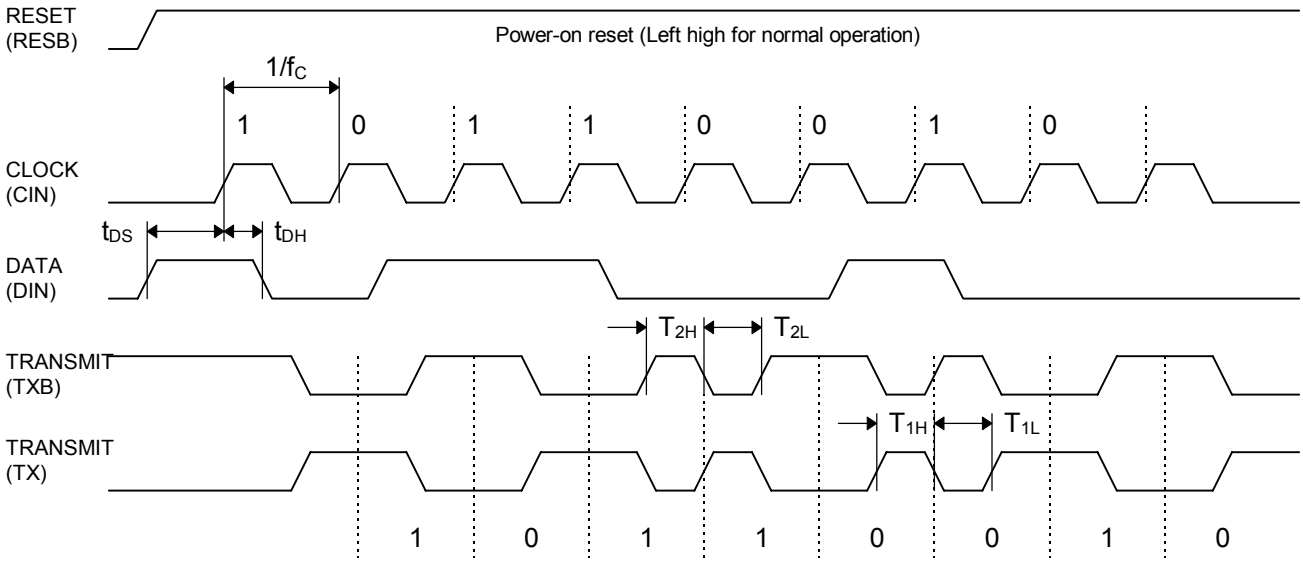


Figure 1: Timing Diagram

DEVICE SPECIFICATIONS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{DD}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Input Pin Current	I_{IN}	-10	10	mA	25C
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 2: DC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 3.0V to 3.6V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Static Supply Current*	I_{DD}		5	mA	
High Level Input Voltage	V_{IH}	2.0		V	
Low Level Input Voltage	V_{IL}		1.0	V	
High Level Input Current	I_{IH}		1.0	µA	$V_{IH} = V_{DD}$
Low Level Input Current	I_{IL}		1.0	µA	$V_{IL} = 0V$
High Level Output Current	I_{OH}		-4.0	mA	$V_{DD} = 3.0V$ $V_{OH} = 2.4V$
Low Level Output Current	I_{OL}	4.0		mA	$V_{DD} = 3.0V$ $V_{OL} = 0.4V$
Output Rise & Fall Time	T_R & T_F		2	ns	C_{LD} = 5 pf

*I_{DD}(Dynamic) = 2 * C_{LD} * V_{DD} * F
where: C_{LD} = Average capacitance load/pin (pf)
F = Input frequency (GHz)

Input Capacitance = 10 pf typical
Output Load Capacitance (C_{LD}) = 25 pf max

TABLE 3: AC ELECTRICAL CHARACTERISTICS

(-40C to 85C, 3.0V to 3.6V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Baud Rate	f_{BN}			50	MBaud	
Clock Frequency	f_C			50	MHz	
Data set-up to clock rising	t_{DS}	3.5			ns	
Data hold from clock rising	t_{DH}	0			ns	
TX High-Low time skew	t_{1H} - t_{1L}	-3.5		3.5	ns	1
TXB High-Low time skew	t_{2H} - t_{2L}	-2.0		2.0	ns	1
TX - TXB High/Low time skew	t_{1H} - t_{2L}	-3.0		3.0	ns	1

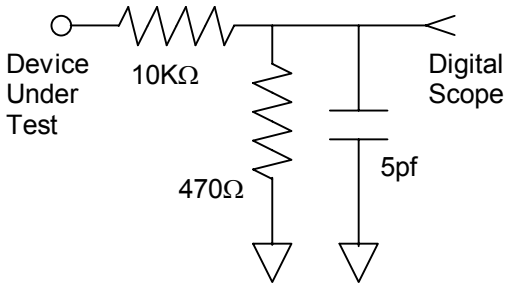
Notes: 1: Assumes a 50% duty cycle clock input

SILICON DELAY LINE AUTOMATED TESTING

TEST CONDITIONS

INPUT:
Ambient Temperature: 25°C ± 3°C
Supply Voltage (Vcc): 5.0V ± 0.1V
Input Pulse: High = 3.0V ± 0.1V
Low = 0.0V ± 0.1V
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured between 0.6V and 2.4V)
Pulse Width: PW_{IN} = 1/(2*BAUD)
Period: PER_{IN} = 1/BAUD

OUTPUT:
R_{load}: 10KΩ ± 10%
C_{load}: 5pf ± 10%
Threshold: 1.5V (Rising & Falling)



NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.

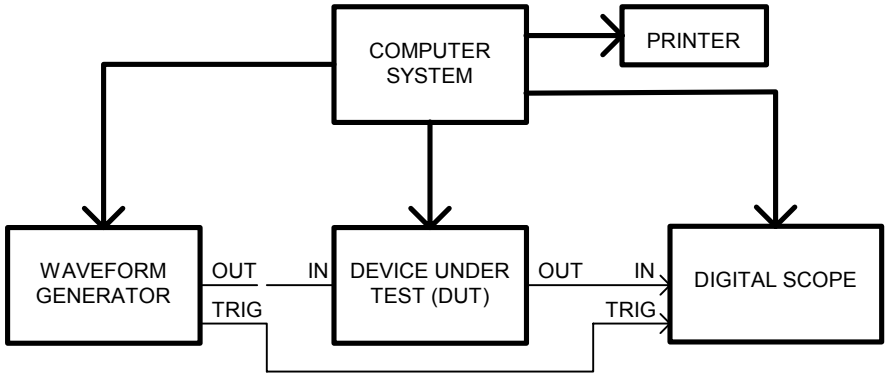


Figure 2: Test Setup

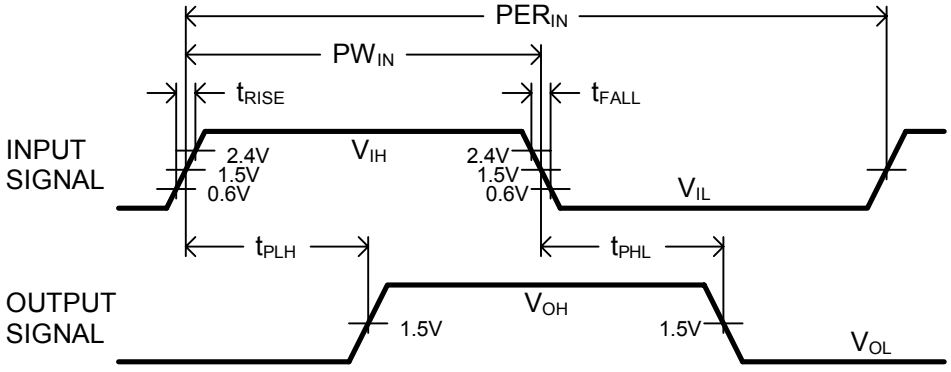


Figure 3: Timing Diagram